In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A method for fabricating a liquid crystal display including a plurality of pixels, the method comprising the steps of:

forming a gate pattern, including a plurality of separated gate lines and a gate electrode array electrically connected with the separated gate lines, in a substrate;

forming a channel array, isolated from the gate electrode array;

forming a source/drain pair array, with the source and drain spaced apart from each other, in the channel array; and

forming a pixel electrode array to connect the drains of the source/drain pair array;

wherein the steps for forming the gate pattern or the source/drain pair array, at least, comprise the steps of:

forming a photoresist layer;

dividing the photoresist layer into a first region, a second region, and a boundary region, divided into a first portion and a second portion by a boundary line, between the first region and the second region;

defining the first region and the first portion with a first mask; and

defining the second region and the second portion with a second mask;

wherein the boundary region corresponds to a sub-array of the gate electrode array or the source/drain pair array; for each row of the gate electrodes or each row of the source/drain pairs in the sub-array, the boundary line is formed in a special pattern; the gate electrodes or the source/drain electrode pairs at the boundary region defined by both of the first and second masks are divided into a first portion patterned by the first mask and a second portion patterned by the second mask; the boundary region is divided incrementally or by square wave such that the area of each of the gate electrodes or the source/drain electrode pairs in the

first portion increases along the boundary direction and that in the second portion decreases along the boundary direction.

2. (Original) The method as claimed in claim 1, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is a tilted straight line.

3. (Original) The method as claimed in claim 1, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in a ladder pattern.

4. (Original) The method as claimed in claim 1, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in a square wave pattern.

5. (Original) The method as claimed in claim 1, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in an embedded line pattern.

6. (Original) The method as claimed in claim 1, wherein the boundary line divides a row of the gate or source/drain electrodes from the first region to the second region, then continues to divide the next row of the gate or source/drain electrodes from the second region to the first region, and so forth.

7. (Original) The method as claimed in claim 1, wherein the boundary line divides a row of the gate or source/drain electrodes from the first region to the second region, then goes back to the first region and continues to divide the next row of the gate or source/drain electrodes from the first region to the second region, and so forth.

8. (Original) A liquid crystal display, wherein the shot mura phenomenon is minimized, is fabricated with the method as claimed in claim 1.

9. (Original) A method for fabricating a liquid crystal display including a plurality of pixels, the method comprising the steps of:

forming a gate pattern, a gate electrode array ,a channel array isolated from the gate electrode array, a source/drain pair array, and a pixel electrode array in a substrate; wherein the gate pattern includes a plurality of separated gate lines connected with the electrode array, and the source and drain in each source/drain pair are spaced from each other, and the pixel electrode array is coupled to the drains of the source/drain pair array;

and wherein the steps for forming the gate pattern and the source/drain pair array, at least, comprise the steps of:

forming a photoresist layer;

dividing the photoresist layer into a first region, a second region, and a boundary region, divided into a first portion and a second portion by a boundary line, between the first region and the second region;

defining the first region and the first portion with a first mask; and

defining the second region and the second portion with a second mask;

wherein the boundary region corresponds to a sub-array of the gate electrode array or the source/drain pair array; for each row of the gate electrodes or each row of the source/drain pairs in the sub-array, the boundary line is formed in a special pattern; the gate electrodes or the source/drain electrode pairs at the boundary region defined by both of the first and second masks are divided into a first portion patterned by the first mask and a second portion patterned by the second mask; the boundary region is divided incrementally or by square wave such that the area of each of the gate electrodes or the source/drain electrode pairs in the first portion increases along the boundary direction and those in the second portion decreases along the boundary direction.

10. (Original) The method as claimed in claim 9, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is a tilted straight line.

11. (Original) The method as claimed in claim 9, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in a ladder pattern.

12. (Original) The method as claimed in claim 9, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in a square wave pattern.

13. (Original) The method as claimed in claim 9, wherein the boundary line used for dividing each row of the gate electrodes and each row of the source/drain pairs is in an embedded line pattern.

14. (Original) The method as claimed in claim 9, wherein the boundary line divides a row of the gate or source/drain electrodes from the first region to the second region, then continues to divide the next row of the gate or source/drain electrodes from the second region to the first region, and so forth.

15. (Original) The method as claimed in claim 9, wherein the boundary line divides a row of the gate or source/drain electrodes from the first region to the second region, then goes back to the first region and continues to divide the next row of the gate or source/drain electrodes from the first region to the second region, and so forth.